Introduction to Digital Logic

EECS/CSE 31L

**Assignment 1**

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**1.1 Assignment Description**

Follow the instructions in the tutorial for each tool appended to this text. CAD tools you will work with

in this assignment are:

**Tool 1:** Questasim® MentorGraphics

**Tool 2:** Incisive Enterprise Simulator from Cadence

**1.2 Assignment Deliverable**

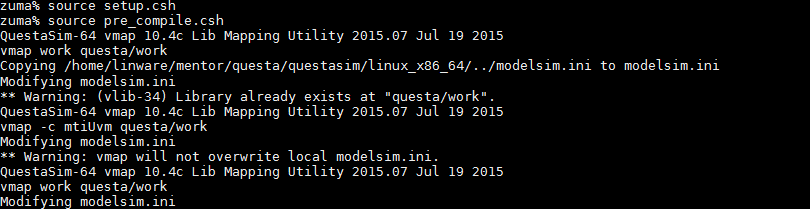
**Tool 1: Questasim® MentorGraphics**

• A short report on what you have learned

What I learned:

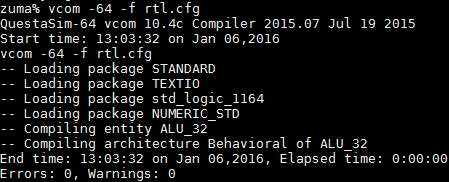
* Questasim can only be used on zuma or crystalcove Unix servers
* How to setup a project that uses Questasim
* Install Questasim for my use on the server for the project
* Compile the VHDL(.vhd) design files and the System Verilog(.sv) testbench files
* Optimize the VHDL design
* Simulate the design
* View the waveform

Questasim installation

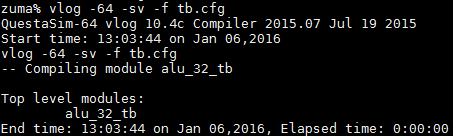


• Compilation, Elaboration, and Simulation logs

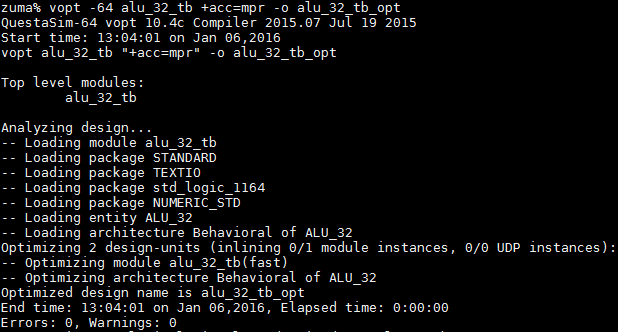
VHDL Design Compilation



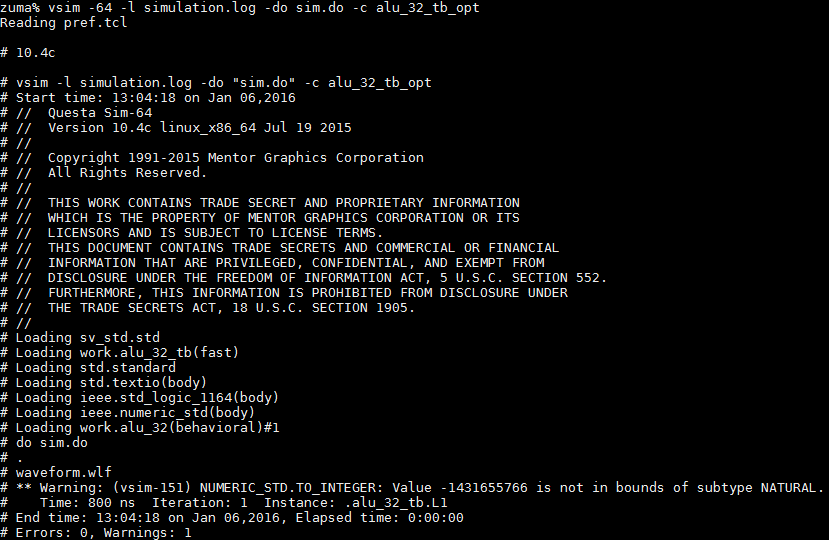
System Verilog Testbench Compilation



VHDL Design Optimization



Simulation Log

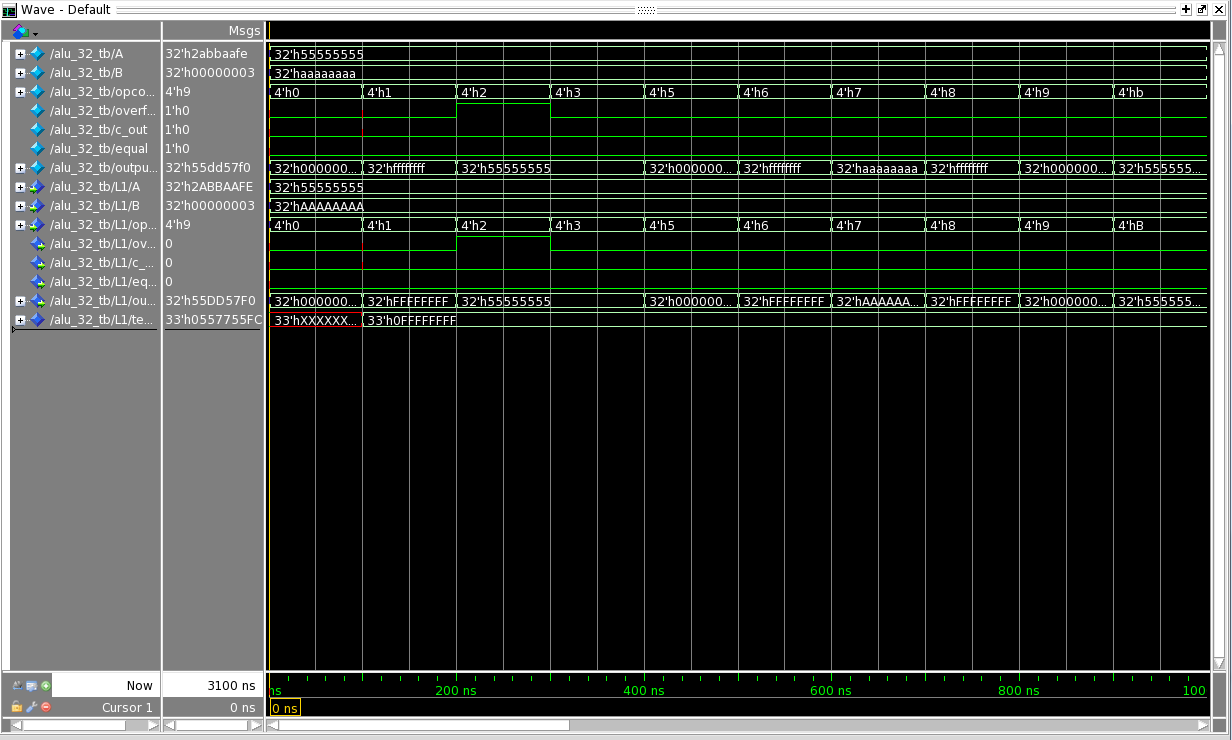


• Waveform snapshot from each tool

Opening waveform



Sample Waveform



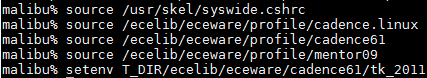
**Tool 2: Incisive Enterprise Simulator from Cadence**

• A short report on what you have learned

What I learned:

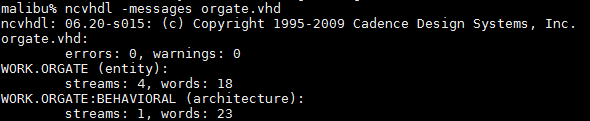
* Cadence can only be used on malibu or vivian Unix servers
* Enable Cadence for use on my account
* How to setup a project that uses Cadence
* Compile the VHDL(.vhd) design files and the System Verilog(.sv) testbench files
* Elaborate the VHDL design
* Simulate the design
* View the waveform

Cadence Installation



• Compilation, Elaboration, and Simulation logs

VHDL Design Compilation



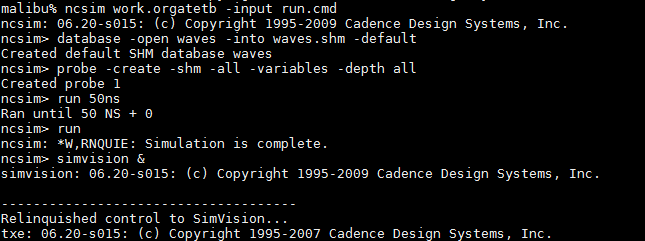
System Verilog Testbench Compilation



VHDL Design Elaboration

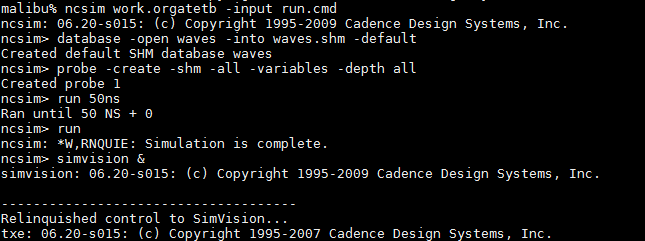


Simulation Log



• Waveform snapshot from each tool

Open Waveform



Waveform Snapshot

